EAST - [thinhsearch15.wsp:1]

File View Edit Tools Window Help

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  - L1: (1) 10/437060
  - L2: (93) sidewall adj select adj gate
  - L3: (279) sidewall adj floating adj gate
  - L4: (20) 2 and 3
  - L5: (131) trench$3 adj floating adj gate
  - L6: (3) dual adj profile$1 adj trench
  - L7: (38669) second adj opening
  - L8: (56107) flash adj memory
  - L9: (183) 7 and 8
  - L10: (0) 5 and 9
  - L11: (59) 9 and trench
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DBs | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB

Default operator: OR

Plurals | Highlight all hit terms initially

9 and trench

BRS form | ISR form | Image | Text | HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Cla	Inventor	S	C	P	2	3	Image 1
1			US 20040137696 A1	20040715	22	Methods of forming semiconductor devices having field oxides in trenche	438/424			Kim, Hong-Soo et al.						US 2004
2			US 20040135184 A1	20040715	58	Nonvolatile magnetic memory device and manufacturing method thereof	257/295			Motoyoshi, Makoto						US 2004
3			US 20040113181 A1	20040617	16	Lateral phase change memory and method therefor	257/246			Wicker, Guy C.						US 2004
4			US 20040051164 A1	20040318	13	Two-transistor pixel with buried reset channel and method of formation	257/595			Fossum, Eric R.						US 2004
5			US 20040046195 A1	20040311	54	Semiconductor integrated circuit device and process for manufacturing	257/296	257/298; 257/306;		Nakamura, Yoshitaka et al.						US 2004
6			US 20040043529 A1	20040304	13	Two-transistor pixel with buried reset channel and method of formation	438/70			Fossum, Eric R.						US 2004
7			US 20040036124 A1	20040226	18	Inverted staggered thin film transistor with salicided source/drain structures	257/382	257/383; 257/384;		Vyvoda, Michael A. et al.						US 2004
8			US 20030219951 A1	20031127	18	Semiconductor constructions, and methods of forming semiconductor c	438/305	438/268		Gonzalez, Fernando						US 2003
9			US 20030219943 A1	20031127	9	METHOD OF FABRICATING A FLOATING GATE FOR SPLIT GA	438/257	257/E21.209; 438/593		Lin, Chi-Hui et al.						US 2003
10			US 20030218208 A1	20031127	19	Split gate flash memory cell and method for fabricating the same	257/316	257/318; 257/E21.692;		Lin, Chi-Hui et al.						US 2003
11			US 20030216001 A1	20031120	32	Non-volatile memory device having a bit line contact pad and method for m	438/258	257/E21.59; 257/E21.682;		Lee, Seung-Min et al.						US 2003
12			US 20030215978 A1	20031120	15	Method for making tapered opening for programmable resistance memory	438/95	257/E45.002		Maimon, Jon et al.						US 2003
13			US 20030181052 A1	20030925	16	Method of forming integrated circuit structures in silicone ladder polymer	438/694	257/E21.026; 257/E21.256;		Rasmussen, Robert						US 2003
14			US 20030134473 A1	20030717	10	Novel process for flash memory cell	438/257			Sung, Hung-Cheng et al.						US 2003
15			US 20030124801 A1	20030703	19	Method for fabricating flash memory cell	438/257			Lin, Chi-Hui						US 2003
16			US 20030100172 A1	20030529	27	Gate-contact structure and method for forming the same	438/585			Kim, Sun-Young et al.						US 2003

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9 and trench

8/09/04

BRS term | ISR form | Image | Text | HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Cla	Inventor	S	C	P	A	3	Image I
1			US 20040137696 A1	20040715	22	Methods of forming semiconductor devices having field oxides in trenche	438/424			Kim, Hong-Soo et al.						US 2004
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